RECEIVED
CENTRAL FAX CENTER
AUG 11 2008

Verification of Translation

U.S. Patent Application No. 10/553860

Title of the Invention:
FIELD EFFECT TRANSISTOR, ELECTRICAL ELEMENT ARRAY, AND MANUFACTURING METHOD FOR THE SAME

I, Shin TANIMURA, whose full post office address is IKEUCHI·SATO & PARTNER PATENT ATTORNEYS, 26th Floor, OAP Tower 8-30, Tenmabashi, 1-Chome, Kita-ku, Osaka-shi, 530-6026, Japan am the translator of the document attached and I state that the following is a true translation to the best of my knowledge and belief of JP 2003-409342.

At Osaka, Japan
Dated this 30/07/2007 (Day/Month/Year)

Signature of the translator

Shin TANIMURA

PATENT OFFICE

JAPANESE GOVERNMENT

This is to certify that the annexed is a true copy of the following application as filed with this Office.

Date of Application: December 8, 2003

Application Number: Patent Application No. JP 2003-409342

Applicant(s): Matsushita Electric Industrial Co., Ltd.

[Document Name] Patent Application
[Case Number] 2047550007
[Date of Application] December 8, 2003
[Destination] Director–General of the Japanese Patent Office
[Intern. Patent Classification] H01L 27/088
H01L 21/70
H01L 29/786
[Inventor]
[Address] c/o Matsushita Electric Industrial Co., Ltd., 1006-banchi, Oaza-kadoma, Kadoma-shi, Osaka-fu
[Name] Norishige NANAI
[Inventor]
[Address] c/o Matsushita Electric Industrial Co., Ltd., 1006-banchi, Oaza-kadoma, Kadoma-shi, Osaka-fu
[Name] Takayuki TAKEUCHI
[Patent Applicant]
[Identification Number] 000005821
[Name/Title] Matsushita Electric Industrial Co., Ltd.
[Attorney]
[Identification Number] 110000040
[Name] Ikeuchi・Sato & Partner Patent Attorneys
[Representative] Hiroyuki IKEUCHI
[Telephone Number] 06-6135-6051
[Indication of Official Fees]
[Deposit Account Number] 139757
[Amount of Deposit] 21000
[List of File Documents]
[Name of Document] Claims 1
[Name of Document] Patent Specification 1
[Name of Document] Drawings 1
[Name of Document] Abstract 1
[General Power of Attorney's Number] 0108331

[DOCUMENT NAME] CLAIMS

[Claim 1]

A thin film transistor comprising a semiconductor including at least nanotube, the semiconductor being disposed on a substrate, wherein the thin film transistor further comprises a protective layer for coating the semiconductor so as to stabilize a semiconductor polarity of the nanotube.

[Claim 2]

The thin film transistor according to claim 1, wherein the protective layer for coating the semiconductor includes polyimine.

[Claim 3]

The thin film transistor according to claim 1, wherein the protective layer for coating the semiconductor includes a polymer other than polyimine.

[Claim 4]

The thin film transistor according to claim 1, wherein the semiconductor including nanotube is an active layer.

[Claim 5]

The thin film transistor according to claim 1, wherein the nanotube is carbon nanotube.

[Claim 6]

An electrical element array comprising a plurality of semiconductors including nanotube, the plurality of semiconductors being disposed on a substrate, wherein the electrical element array further comprises a protective layer for coating the semiconductors so as to stabilize a semiconductor polarity of the nanotube.

[Claim 7]

The electrical element array according to claim 6, wherein the semiconductors including nanotube are active layers.

[Claim 8]

The electrical element array according to claim 6, wherein the nanotube

is carbon nanotube.

[Claim 9]

A method of manufacturing a thin film transistor comprising a semiconductor including at least nanotube, the semiconductor being disposed on a substrate, the thin film transistor further comprising a protective layer for coating the semiconductor so as to stabilize a semiconductor polarity of the nanotube,

wherein a step of forming the protective layer for coating the semiconductor also serves as a step of converting the semiconductor polarity of the nanotube.

[Claim 10]

The method of manufacturing a thin film transistor according to claim 9, wherein the protective layer for coating the semiconductor is formed by an ink-jet method.

[Claim 11]

An electronic apparatus comprising a circuit device using the thin film transistor or the electrical element array according to any of claims 1 to 8.

[DOCUMENT NAME] SPECIFICATION

[TITLE OF THE INVENTION] THIN FLIM TRANSISTOR, ELECTRICAL ELEMENT ARRAY, MANUFACTURING METHOD FOR THE SAME, AND ELECTRONIC APPARATUS

[Technical field to which the invention pertains]

[0001]

The present invention relates to thin film field effect transistors or thin film transistors (TFTs), and particularly relates to TFTs and electrical element arrays using a semiconductor layer including nanotube, and a manufacturing method for the same.

[Prior art]

[0002]

Currently, in thin film field effect transistors or thin film transistors (TFTs) used in the field of flat panel displays, the switching between a source electrode and a drain electrode, isolated from each other by a semiconductor in which a channel is defined intervening therebetween, is controlled by a voltage applied to a gate electrode. TFT devices that have become commercially practical employ amorphous silicon (a-Si) or low-temperature polysilicon as the semiconductor and silicon oxide or silicon nitride as a gate insulation layer. In order to manufacture a device such as a display based on these technologies, a manufacturing process at high temperature has been required often.

[0003]

Meanwhile, along with the development of technologies for flat panel displays, there have been further demands for a lighter substrate with mechanical flexibility, impact resistance and resource saving. However, a plastic board and a resin film effective for these demands have constraints when they undergo the manufacturing process at temperatures exceeding 200°C.

[0004]

In recent years, organic semiconductor thin film transistors (organic TFTs) also have been researched, which use organic materials showing semiconductor properties. The use of the organic materials permits thin film devices to be manufactured by a process at further lower temperature than those of a conventional a-Si and low-temperature polysilicon. Therefore, it can be expected that thin film devices can be manufactured without preparing facilities at high cost that are required for a process using silicon-based materials. Further, the manufacturing without high temperature steps facilitates the usage of a plastic board and a resin film having mechanical flexibility as a substrate, which may lead to the realization of displays and mobile equipment that are like a sheet or paper.

[0005]

In the case of organic TFTs using low-molecular organic semiconductor such as pentacene, the carrier mobility of a channel is smaller than that of a low-temperature polysilicon-based semiconductor layer, whose value is about 0.1 to 3 cm^2/Vs (for example, non-patent document 1). However, when the crystalline interface increases or crystallinity deteriorates, the carrier mobility is decreased, resulting in a failure in practical use as TFTs.

[0006]

To cope with this, TFTs (CNT-TFTs) using carbon nanotube (CNT) as a semiconductor layer also have been reported, the carbon nanotube having a nano structure, made of carbon and having significantly excellent conductivity and toughness properties. The CNT-TFTs have large carrier mobility, and about 1,000 to 1,500 cm^2/Vs has been obtained (for example, non-patent document 5). Taking advantage of this large carrier mobility of CNT, patent document 1 proposes to utilize CNT for FETs.

[0007]

It is known that once CNT-TFTs are exposed to the air, they show p-type characteristics. They can be converted into n-type by vacuum heating or a treatment with alkali metal. However, when they are exposed to oxygen or

water, they return to p-type (non-patent document 2). Non-patent document 3, however, proposes that n-type CNT-FETs stable even in the air can be manufactured by treating CNT with an imine-based polymer such as polyethylene-imine.

[0008]

When CNT is used as the semiconductor of TFTs, it is preferable that both of p-type and n-type can be manufactured on the same substrate in terms of the circuit design. Non-patent document 4 proposes two methods of arranging p-type and n-type CNTs on the same substrate so as to manufacture a logical NOT circuit (NOT gate). One of the methods proposed by non-patent document 4 follows: in a circuit prepared by arranging CNTs at predetermined positions of a substrate, a pattern for TFTs that should be n-type is applied with a photolithographic resin for protection, followed by vacuum heating at 200°C for 10 hours so that all of the CNT-TFTs are turned into n-type once. Subsequently, this is exposed to 10^{-3} Torr of oxygen for 3 min., so that the TFTs unprotected by the resin are turned into p-type so as to manufacture a NOT gate. The other method proposed by non-patent document 4 follows: in a circuit prepared by arranging CNTs at predetermined positions of a substrate, a pattern for TFTs that should be p-type is applied with a photolithographic resin for protection, followed by evaporation of potassium so as to turn the TFTs unprotected by the resin into n-type, thus manufacturing a NOT gate.

[0009]

Meanwhile, Patent document 1 does not describe that optional CNTs, which are required in manufacturing an array in which p-type and n-type CNTs are intermixed, are controlled to form separately p-type and n-type CNTs.

[Patent document 1] JP 2003-17503 A

[Non-patent document 1] C.D.Dimitrakopoulos et al. J. Appl. Phys. 80, pp.2501-2508 (1996)

[Non-patent document 2] V.Derycke et al. Appl. Phys. Lett. 80, pp.2773-2775 (2002)

[Non-patent document 3] Moonsub Shim et al. J. Am. Chem. Soc. 123, pp.11512-11513 (2001)

[Non-patent document 4] V.Derycke et al. Nano Lett. 1, pp.453-456 (2001)

[Non-patent document 5] S.Rosenblatt et al. Nano Lett. 2, pp.869-872 (2002)

[Disclosure of the Invention]

[Problem to be solved by the invention]

[0010]

As stated above, in order to manufacture a circuit including p-type and n-type CNT-FETs on the same substrate, a process for converting the characteristics between p-type/n-type is required in addition to a complicated process of applying a pattern by photolithography for protection, as proposed by non-patent document 4. Further, in the case where CNTs are turned into n-type using metal such as potassium, there is a need to control the amount of evaporation of potassium in order to reduce a leakage current between a source electrode and a drain electrode. In addition, although not mentioned by non-patent document 4, when the conversion into n-type is carried out using potassium, following the patterning by photolithography for protection, protective coating from the air is required as is evident from non-patent document 2. In this way, according to the conventional methods for manufacturing a circuit including p-type and n-type CNT-FETs on the same substrate, the device has to undergo a time-consuming process of vacuum heating for a long time so as to manufacture n-type CNTs, or some measure for reducing a leakage current has to be devised for the case of using metal such as potassium. As additional problems, a complicated process as a whole including patterning, conversion of characteristics and sealing is required.

[0011]

In order to cope with these conventional problems, the present invention provides a method of manufacturing a circuit including p-type and n-type CNT-FETs on the same substrate by a simpler process than conventionally, and thereby provides a thin film transistor and an electrical element array that are stable in the air, a manufacturing method for the same, and an electronic apparatus.

[Means for solving problem]

[0012]

The thin film transistor of the present invention includes a semiconductor including at least nanotube, the semiconductor being disposed on a substrate, and a protective layer for coating the semiconductor layer so as to stabilize the semiconductor polarity of the nanotube.

[0013]

The electrical element array of the present invention includes a plurality of semiconductors including nanotube, the plurality of semiconductors being disposed on a substrate, and a protective layer for coating the semiconductors so as to stabilize the semiconductor polarity of the nanotube.

[0014]

The method of manufacturing a thin film transistor of the present invention is a method of manufacturing a thin film transistor comprising a semiconductor including nanotube, the semiconductor being disposed on a substrate, and a protective layer for coating the semiconductor so as to stabilize the semiconductor polarity of the nanotube. A step of forming the protective layer for coating the semiconductor also serves as a step of converting the semiconductor polarity of the nanotube.

[0015]

The electronic apparatus of the present invention includes a circuit device using the thin film transistor or the electrical element array.

[Effects of the invention]

[0016]

According to the present invention, by providing an electrical element that includes a semiconductor including at least nanotube, the semiconductor being disposed on a substrate, and a protective layer for coating the semiconductor so as to stabilize the semiconductor polarity of the nanotube, a circuit including p-type and n-type CNT-FETs on the same substrate can be manufactured more simply than by the conventional techniques, and a CNT-FET circuit that is stable in the air can be provided.

[Embodiments of the invention]

[0017]

The present invention provides an electrical element that includes a semiconductor including at least nanotube, the semiconductor being disposed on a substrate, and a protective layer for coating the semiconductor so as to stabilize the semiconductor polarity of the nanotube. Thus, a circuit including p-type and n-type CNT-FETs on the same substrate can be manufactured by a simpler process than conventionally, and a CNT-FET circuit that is stable in the air can be provided. It is preferable that the protective layer for coating the semiconductor includes an imine compound. Further, it is preferable that the protective layer for coating the semiconductor includes a high polymer compound. An example of the electrical element includes a transistor in which the semiconductor including nanotube is an active layer. An example of the nanotube includes carbon nanotube.

[0018]

The present invention provides an electrical element array that includes a plurality of semiconductors including nanotube, the plurality of semiconductors being disposed on a substrate, and a protective layer for coating the semiconductors so as to stabilize the semiconductor polarity of the nanotube.

[0019]

As a way to obtain the electrical element or the electrical element array, there is a manufacturing method in which a step of forming the protective layer for coating the semiconductor also serves as a step of converting the semiconductor polarity of the nanotube. An examples of the step of forming the protective layer for coating the semiconductor includes an ink-jet method.

[0020]

Note here that the configurations of the above-described means can be combined mutually without departing from the spirit or essential characteristics of the present invention.

[0021]

The following describes an embodiment of the present.invention.

[0022]

(Embodiment 1)

The following exemplifies as an embodiment of the present invention in the case where a NOT gate is manufactured.

[0023]

Fig. 1A schematically shows an exemplary circuit (NOT gate) in cross section configured with thin film transistors of Embodiment 1 of the present invention, and Fig. 1B is a circuit diagram of the same. Reference numeral 101 denotes a substrate, and 102 denotes a gate electrode of p-type and n-type TFTs in the circuit, which functions as an input of the NOT gate. A voltage input to the input electrode 102 enables the switching between a p-type semiconductor layer 105 and an n-type semiconductor layer 108 so as to output either of the voltages of a positive power supply electrode 106 and a negative power supply electrode 109 to an output electrode 104. The gate electrode 102 is isolated from other electrodes and semiconductor layers by a gate insulation layer 103. The p-type semiconductor layer 105 and the n-type semiconductor layer 108 are protected by a p-type semiconductor

protective layer 107 and an n-type semiconductor protective layer 110, respectively.

[0024]

The circuit shown in Fig. 1A and 1B is manufactured on the substrate in accordance with the manufacturing process shown in Fig. 2. The gate electrode, the gate insulation film, the positive and the negative power supply electrodes, and the output electrode are laminated and patterned on the substrate. Although the gate insulation film preferably is thinner within a range not causing the shortage of a withstand voltage, the thickness of SiO_2 as the gate insulation film in this example was set at 100 nm for reasons of the manufacturing. A distance between the positive and the negative power supply electrodes and the output electrode was set at 1 μm in this example for reasons of the manufacturing, but this can be set freely as long as patterning is possible. Although a width of the output electrode was set at 50 μm in this example for reasons of the wiring, FETs can operate with a thinner electrode width as well. As the substrate, polyimide of 0.5 mm in thickness was used. As the respective electrodes of the gate, the positive power supply and the negative power supply, gold of 30 μm in thickness was used, whose thickness was made thinner at portions contacting with CNTs. Next, CNT was dispersed in a solvent, and was applied and dried. Although dichloromethane is selected as the solvent in this example, other solvents can be used as well as long as carbon nanotube (CNT) can be dispersed therein. The concentration in this example was set at 2 mass%, but the concentration can be selected freely as long as it allows the arrangement of CNT on the electrodes. CNT was dispersed by applying ultrasonic waves for 5 min. using an ultrasonic cleaner. In this way, 401 that is a state in which the electrodes, the insulator and the semiconductor are provided on the substrate is obtained. Next, an ink containing 7 mass% of polymethyl methacrylate (PMMA; average molecular weight of 46,000 to 93,000) as a protective agent of the p-type CNT-FET

semiconductor dissolved in toluene and an ink containing 6 mass% of polyethylene-imine (average molecular weight of 10,000) as a protective agent of the CNT-FET semiconductor whose characteristics are converted into n-type dissolved in methanol were prepared. These inks are applied separately as a p-type semiconductor protective layer 404 and an n-type semiconductor protective layer 405, respectively, using an ink-jet printing method. At this time, the n-type semiconductor protective layer is formed and at the same time the conversion of the characteristics into n-type is carried out. Therefore, no particular process for converting the characteristics is required. Both of the p-type semiconductor protective layer and the n-type semiconductor protective layer had a thickness of 6 to 12 μm after drying. In this example, although the ink-jet printing method was selected as a simple technique for applying the semiconductor protective agents at the respective selected positions, any printing method for enabling such selective application or the like can be used for manufacturing. According to this embodiment, the semiconductor characteristics of the CNT are converted concurrently with the formation of the semiconductor protective layers, whereby the manufacturing process can be simplified. Finally, a protective layer 403 was provided for protecting the entire device, so that a circuit configured with the CNT-FETs could be obtained. As the protective layer 403, a photocurable polyimide resin for passivation film ("Pimel") is used.

[0025]

With respect to the thus obtained NOT gate, +2.4 V was applied to the positive power supply electrode 106 and −2.4 V was applied to the negative power supply electrode 109. When +4 V was applied to the input electrode 102, the voltage of the output electrode was −1.6 V. When −4 V was applied to the input electrode, the voltage of the output electrode was +1.6 V. In this way, the polarities of the input and the output were reversed, thus realizing a logical NOT operation. Herein, the absolute value of the output

voltage was smaller than the absolute value of the input voltage because the gate insulation film was too thick in this example.

[0026]

Since the NOT gate circuit operated normally for the positive and negative inputs, it was found that both of the p-type and the n-type CNT-FETs configuring the circuit functioned and p-type and n-type characteristics were assigned to the CNT-FETs by the semiconductor protective layers 404 and 405. This is because if two CNT-FETs configuring a circuit have the same polarity, then they can operate normally for input of one polarity, but the output will be substantially 0 V for the opposite polarity.

[0027]

In this Embodiment 1, the NOT gate is exemplified as the circuit. However, since this example allows a circuit including p-type and n-type FETs on the same substrate and stable in the air to be manufactured simply, the circuit is not limited to a NOT gate. In addition to logical NOT, this example is applicable to logical OR, AND, and a logical circuit equal to the combination of them as well as a part of a display circuit that is incorporated as a switching circuit into a matrix-type panel and an information recording or information reading circuit. This embodiment shows a manufacturing method particularly favorable for providing many TFT elements on a single substrate, and therefore is particularly effective for manufacturing circuits for these.

[0028]

In this Embodiment 1, PMMA was used as the semiconductor protective layer of CNT-TFTs. However, since PMMA does not contribute to the determination of polarity, this can be substituted with the protective layer 403 so that the protective layer 403 doubles as that function. The provision of the semiconductor protective layer, which does not contribute to the determination of polarity, is preferable in order to take advantage of its

buffering function, which protects the semiconductor from mechanical and thermal stress occurring during the lamination of the protective layer 403 and protects the semiconductor from mechanical and thermal stress occurring during the operation or storage of the device.

[0029]

In this embodiment, since p-type CNT treated in the air was used, PMMA was used as the protective layer for the p-type CNT-TFT. However, in the case where CNT converted into n-type by vacuum heating, an alkali metal/ alkaline-earth metal treatment or a treatment with a nitrogen-containing functional group such as imine and imide is used, PMMA can be used as the protective layer of the n-type CNT-TFT as well. This is because PMMA does not contribute to the determination of polarity.

[0030]

Although PMMA was used as a protective layer in this embodiment, any resin that does not contribute to the determination of polarity can exert similar effects. For instance, polycarbonate, polystyrene, polyacrylonitrile, polyvinylidene fluoride, polyvinylidene cyanide, polyvinyl alcohol and the like, and a resin available as the gate insulation film can be used for this purpose. Further, a resin capable of forming a charge-transfer complex with CNT so as to convert the CNT into p-type is possible as the p-type semiconductor protective layer.

[0031]

Although polyethylene-imine [$-(CH_2-C(CH=NH)H)_n-$] (where n represents the polymerization degree) was used in this embodiment as the semiconductor protective layer that converts the characteristics of the CNT into n-type semiconductor, other imine-based resins can be used as well. Among the imine-based resins, polyethylene-imine is preferable because it is mass-manufactured and is easily available. However, polyalkylene imine such as polypropylene imine and polybutylene imine and other imine-based resins can be used as well.

[0032]

Although the protective layer 403 was provided in this embodiment, FETs can operate without the protective layer 403. Therefore, in the case where the circuit is configured in a device including other components besides the circuit, the protective layer 403 can be omitted, and the omission can be compensated with protection for the entire device. The provision of the protective layer 403 is preferable because this layer can prevent the deterioration of FETs caused by mechanical action from the outside and the inside of the device, thermal action due to for example a difference in thermal expansion coefficient between elements configuring the device, action by chemical substances intruding from the environment or included in the device configuration.

[0033]

Although polyimide was used as the substrate in this embodiment, polyester such as polyethylene terephthalate and polybutylene terephthalate and other flexible substrates can be used as well, or not-flexible substrates such as glass and silicon can be used as well. The spirit of this embodiment is that any material can be used as the substrate, as long as devices can be formed thereon.

[0034]

Although gold was used as the electrodes in this embodiment, a laminated structure including other metals such as titanium is possible in order to enhance the adherence with the substrate, or metals other than gold such as chromium, cobalt and nickel also can be used as the electrodes. Further, instead of metal, conductive polymers such as polythiophene and polypyrrole and a charge-transfer complex such as TTF-TCNQ also can be used. Further, the materials of the respective electrodes may be made different from each other and other material layers may be provided for enhancing the interface junction between the semiconductor and the electrodes, and the thicknesses of the electrodes are not limited especially,

and these factors do not affect the spirit of this embodiment.

[0035]

The CNT-FET of this embodiment was exemplified as a thin film transistor including a gate insulation layer, a semiconductor layer provided contacting with the gate insulation layer, a gate electrode contacting with the gate insulation layer and not with the semiconductor layer, a source electrode and a drain electrode provided contacting with at least one side of the semiconductor layer and sandwiching the gate electrode therebetween, which is a bottom-gate thin film transistor whose gate electrode is provided on the substrate. However, a top-gate type thin film transistor similarly can be embodied, whose gate electrode is provided on the opposite side of the substrate relative to the semiconductor layer, and the arrangement of the electrodes does not affect the spirit of this embodiment.

[0036]

(Comparative Example 1)

The following describes a conventional manufacturing method as a comparative example, in accordance with Fig. 3. This method is based on the method proposed by non-patent document 4.

[0037]

Similarly to Embodiment 1, a state 201 in which an electrode, an insulator and a semiconductor are provided on a substrate is obtained. Next, PMMA was applied as resist on 201, followed by exposure, curing and removal so as to provide a protective mask 202 against dopant. Herein, 202 is provided at positions corresponding to CNT-FETs that would be n-type. Subsequently, this was left standing in vacuum at 200°C for 10 hours so as to turn all of the CNT from p-type into n-type. Then, when this was exposed to the air out of the vacuum, the CNT unprotected by the protective mask against dopant 202 is converted from n-type into p-type. The dopant in this case was oxygen in the air.

[0038]

In this way, a protective layer 203 was provided after a circuit with the p-type and n-type CNT-FETs arranged therein was obtained. As described above, since Comparative Example 1 required the process for converting the characteristics twice, the number of the steps increased as compared with that of Embodiment 1. While Embodiment 1 allowed the conversion of the characteristics to be performed concurrently with the step for manufacturing a protective mask, the step for converting into n-type of Comparative Example 1 took a relatively long time. From these points, it was understood that Embodiment 1 allowed a circuit including p-type and n-type CNT-FETs on the same substrate to be manufactured more simply than Comparative Example 1.

[0039]

(Comparative Example 2)

The following describes as a comparative example a conventional manufacturing method, different from Comparative Example 1, in accordance with Fig. 4. This method is based on the method proposed by non-patent document 4.

[0040]

Similarly to Embodiment 1, a state 301 in which an electrode, an insulator and a semiconductor are provided on a substrate is obtained. Next, PMMA was applied as resist on 301, followed by exposure, curing and removal so as to provide a protective mask against dopant 302 . Herein, unlike Comparative Example 1, 302 was provided at positions corresponding to CNT-FETs that would be p-type. Subsequently, potassium was evaporated thereon under vacuum so as to conduct the conversion from p-type into n-type. Herein, the FETs provided with 302 remained p-type. Note here that although this comparative example used potassium as a dopant in accordance with non-patent document 4, other alkali metals, calcium and the like can be used similarly. Herein, if the evaporation amount of metal as the dopant was excessive, a current will flow through

the dopant metal, which will cause an increase in OFF current of the CNT-FETs. For that reason, the evaporation amount of the dopant should be minimized.

[0041]

After a circuit with the p-type and n-type CNT-FETs arranged therein was obtained as described above, a protective layer 303 was provided. In this way, Comparative Example 2 enables the shortening of the process for converting the characteristics as compared with Comparative Example 1. However, the number of the steps in Comparative Example 2 was larger than that of Embodiment 1 because the step for converting the characteristics was required. This is because Embodiment 1 allowed the conversion of the characteristics to be performed concurrently with the step for manufacturing a protective mask. Further, in the step for conducting the conversion into n-type of Comparative Example 2, compounds such as alkali metals and calcium were used, which could not be handled in the air. On the contrary, the compounds used in Embodiment 1 can be handled in the air. From these points, it was understood that Embodiment 1 allowed a circuit including p-type and n-type CNT-FETs on the same substrate to be manufactured more simply than Comparative Example 2.

[Industrial applicability]

[0042]

The present invention is applicable to various electronic apparatuses: such as a display like sheet or paper-form using switching elements, a driving circuit, a control circuit and the like; mobile equipment using a semiconductor circuit device; disposable equipment such as wireless IC tag; recording equipment or other electronic equipment, as well as to other industrial fields. Therefore, industrial applicability of the present invention is significantly extensive and large.

[Brief description of the drawings]

[0043]

[Fig. 1] Fig. 1A is a diagram showing a schematic cross sectional view of an exemplary circuit configured with a thin film transistor in Embodiment 1 of the present invention, and Fig. 1B is a circuit diagram of the same.

[Fig. 2] Fig. 2 is a schematic view of a manufacturing process of the thin film transistor in Embodiment 1.

[Fig. 3] Fig. 3 is a schematic view of a manufacturing process of a thin film transistor as shown in conventional example 1.

[Fig. 4] Fig. 4 is a schematic view of a manufacturing process of a thin film transistor as shown in conventional example 2.

[Explanation of letters and numerals]

[0044]

101 substrate

102 input electrode (gate electrode)

103 gate insulation layer

104 output electrode

105 p-type semiconductor layer

106 positive power supply electrode

107 p-type semiconductor protective layer

108 n-type semiconductor layer

109 negative power supply electrode

110 n-type semiconductor protective layer

201, 301, 401 state in which an electrode, an insulator and a semiconductor are provided on a substrate

202, 302 protective mask against dopant

203, 303, 403 protective layer

404 p-type semiconductor protective layer

405 n-type semiconductor protective layer

[DOCUMENT NAME] ABSTRACT

[Abstract]

[Objects] The present invention provides a manufacturing method for a circuit including p-type and n-type carbon nanotube (CNT)-thin film transistors (FETs) on the same substrate, and thereby provides a thin film transistor and an electrical element array that are stable in the air, a manufacturing method for the same, and an electronic apparatus.

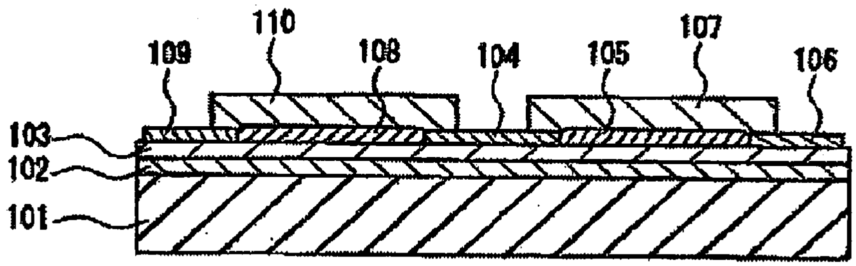
[Means] The thin film transistor of the present invention includes a semiconductor (401) including at least nanotube, the semiconductor being disposed on a substrate, and a protective layer (403) for coating the semiconductor so as to stabilize the semiconductor polarity of the nanotube. By carrying out the conversion of the semiconductor characteristics of the CNT concurrently with the formation of the semiconductor protective layer (403), the process can be simplified. As a result, a CNT-FET circuit that is stable in the air can be provided.

[Selected figure] Fig. 2

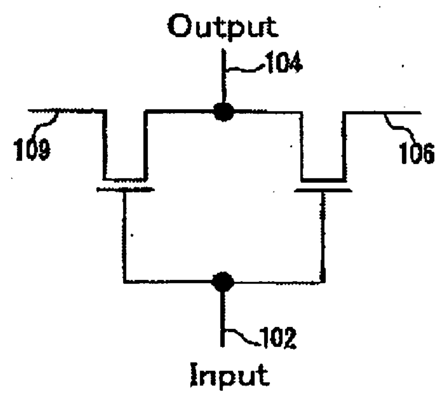
[DOCUMENT NAME] DRAWINGS

[FIG. 1]

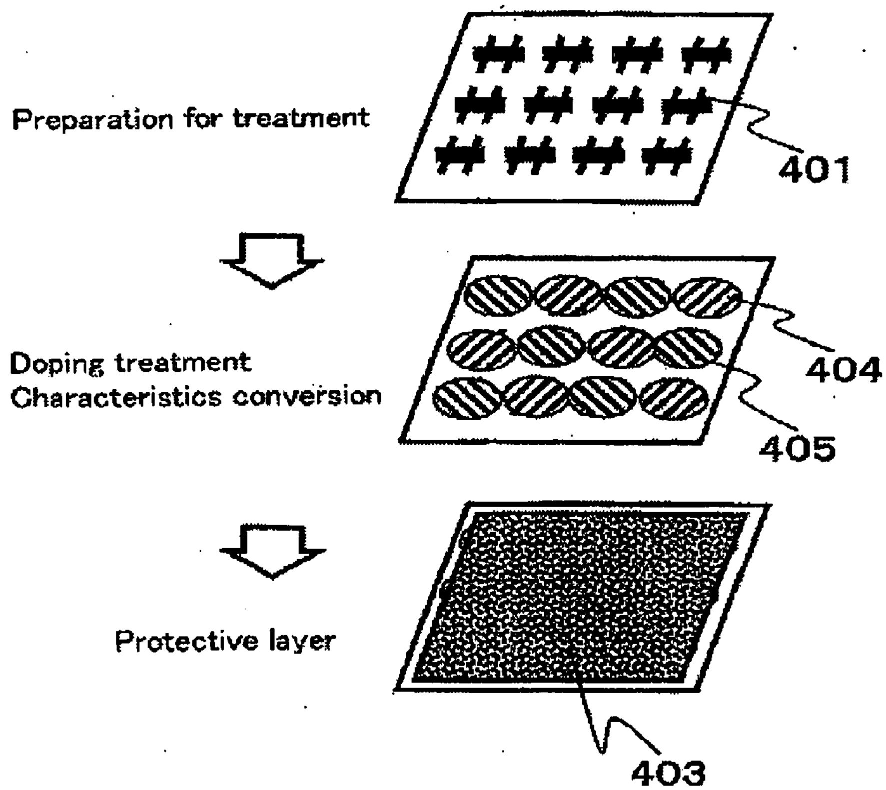
A



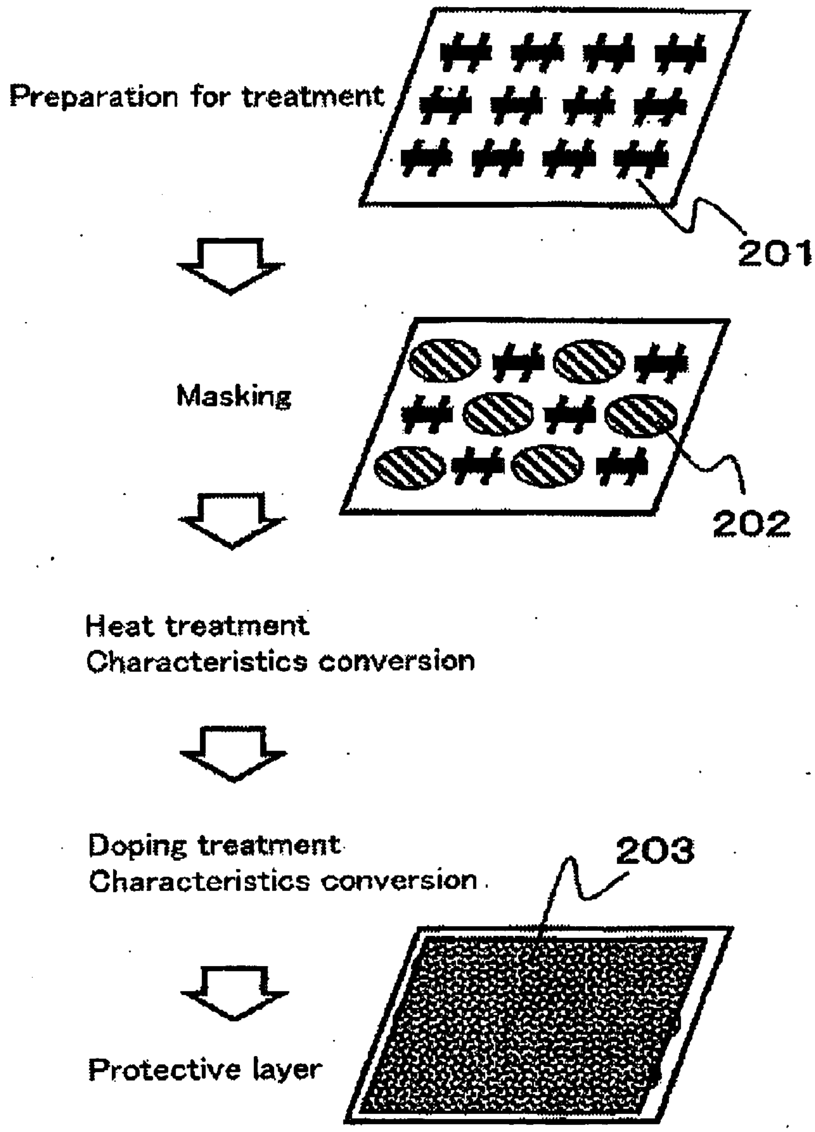
B



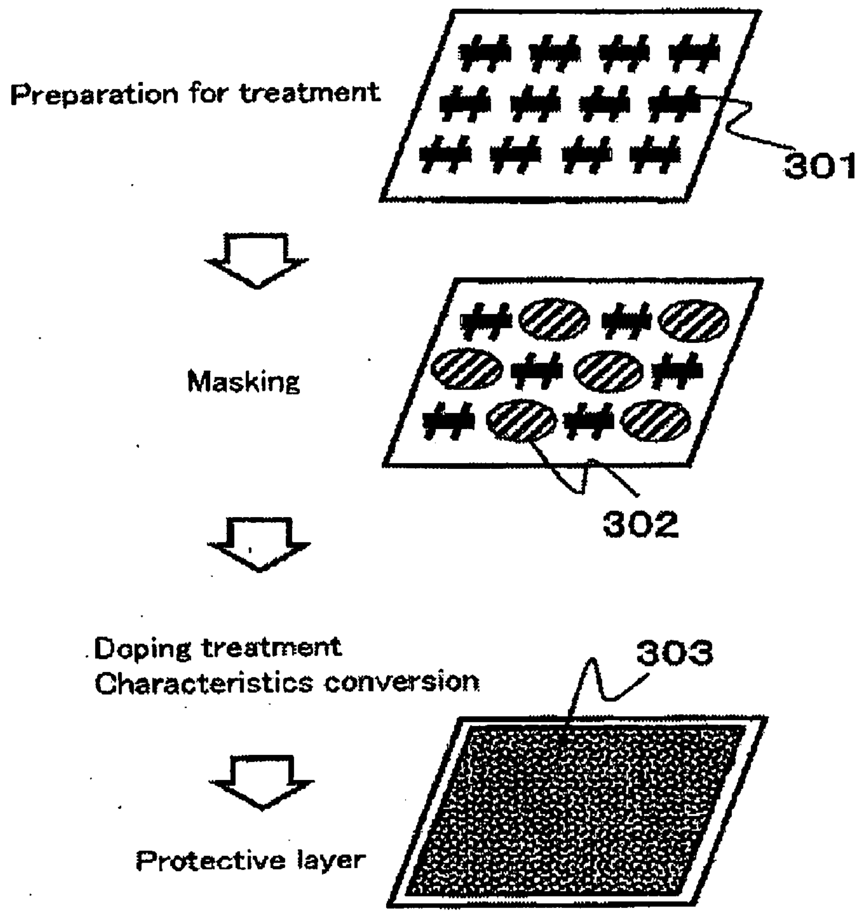
[FIG. 2]


Preparation for treatment
401
Doping treatment
Characteristics conversion
404
405
Protective layer
403

[FIG. 3]


Preparation for treatment
201
Masking
202
Heat treatment
Characteristics conversion
Doping treatment
Characteristics conversion
203
Protective layer

[FIG. 4]


Preparation for treatment
301
Masking
302
Doping treatment
Characteristics conversion
303
Protective layer